

FIG.1A

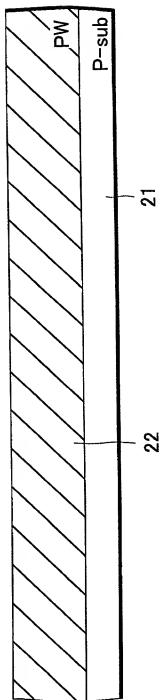


FIG.1B

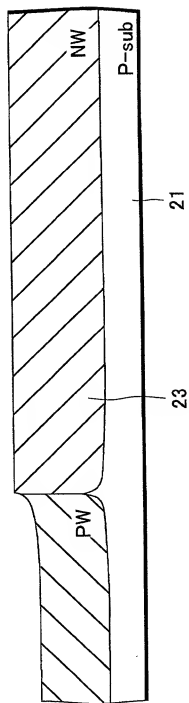


FIG.3A

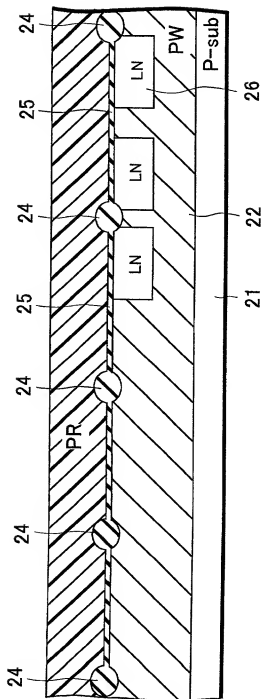


FIG.3B

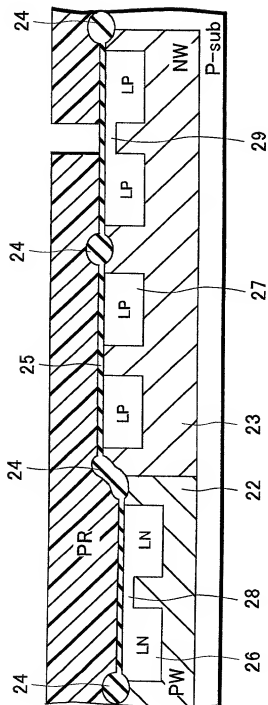


FIG. 4A

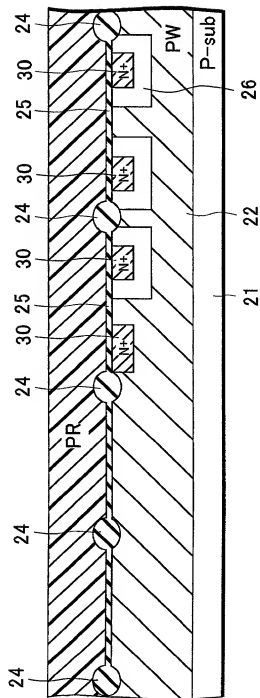


FIG. 4B

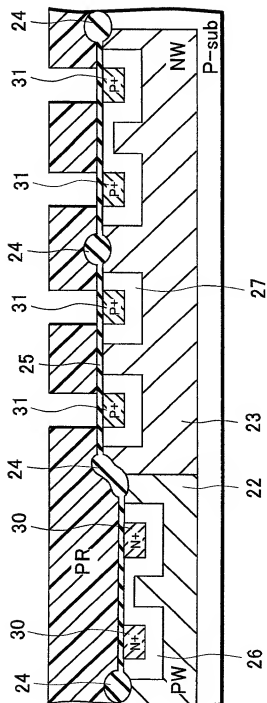


FIG.5A

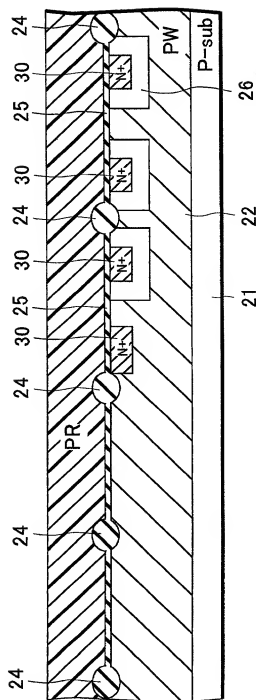


FIG.5B

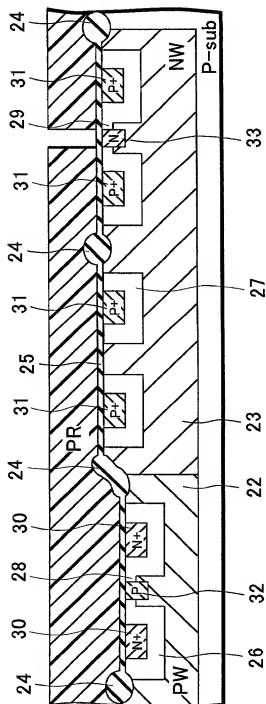


FIG.6A

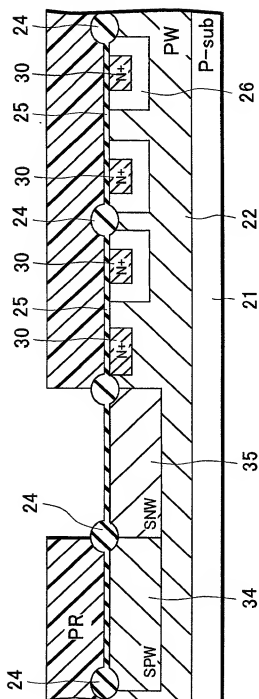


FIG.6B

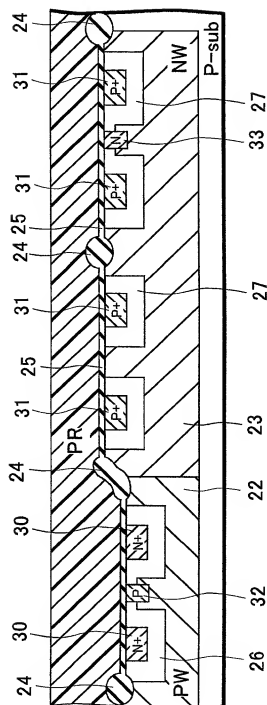


FIG. 7A

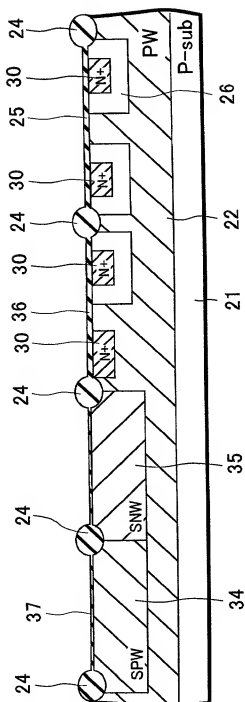
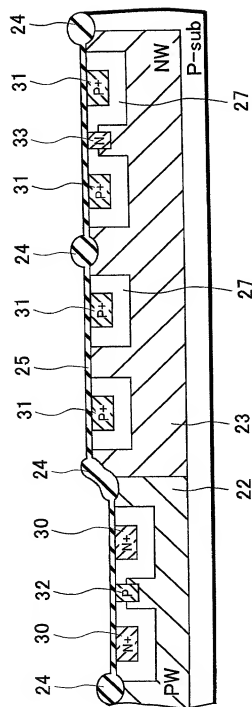


FIG. 7B



This cross-sectional view shows a semiconductor device with a substrate 30. The substrate has a P-sub region 30 and a P-well region PW. A series of gate structures are formed on the substrate, each consisting of a gate stack 24 and a gate contact 38. The gate stacks are labeled 38A, 38B, 38C, and 38D. The gate contacts are labeled 24. The gate stacks 38A and 38B are formed on a source/drain region SPW. The gate stacks 38C and 38D are formed on a source/drain region SNW. The gate stacks 38A and 38B are formed on a source/drain region SPW. The gate stacks 38C and 38D are formed on a source/drain region SNW. The gate stacks 38A and 38B are formed on a source/drain region SPW. The gate stacks 38C and 38D are formed on a source/drain region SNW.

FIG.9A

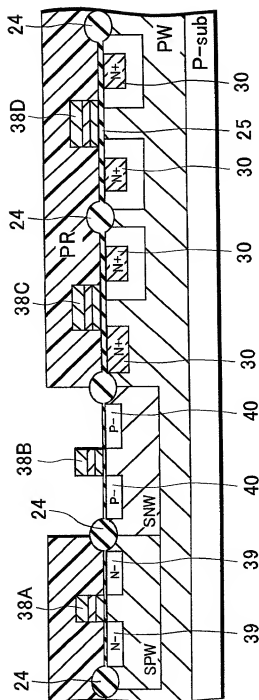


FIG.9B

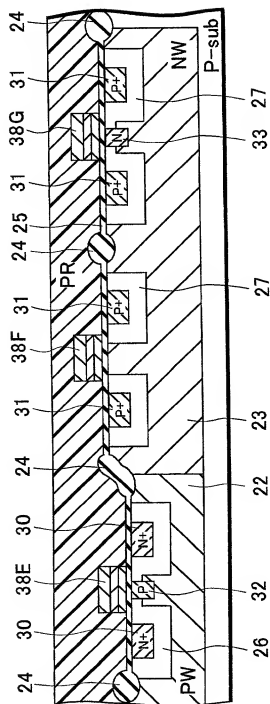


FIG. 10A

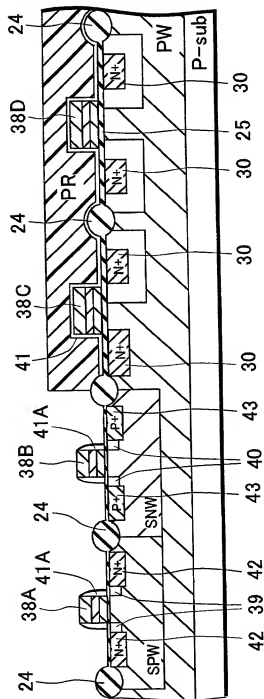


FIG. 10B

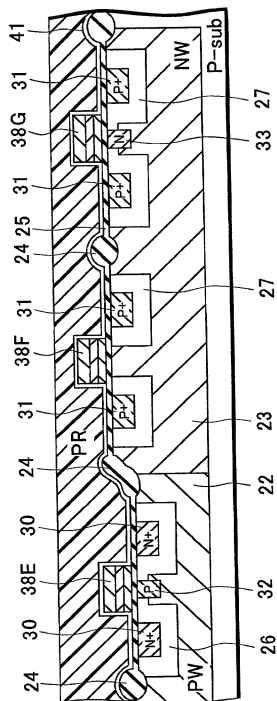


FIG.11

(A) (B) (C)

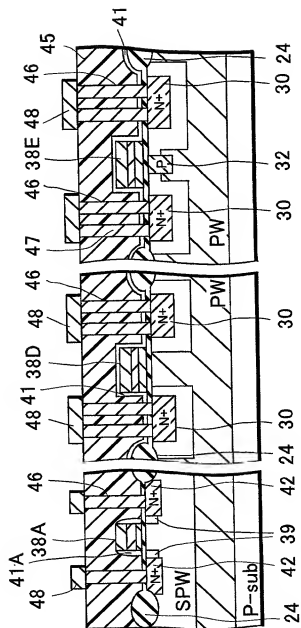


FIG. 12

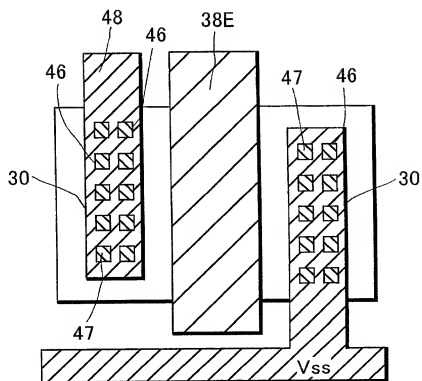


FIG. 13

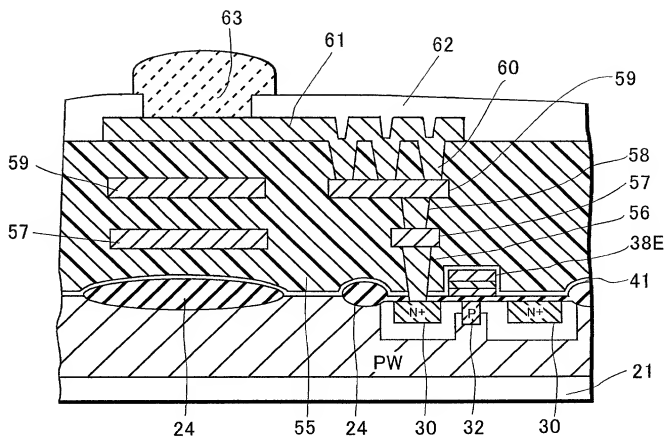


FIG.14

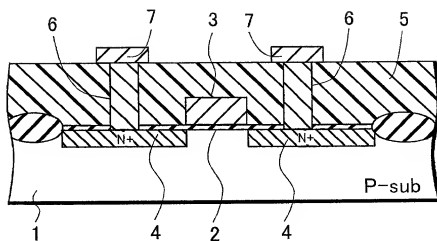


FIG.15

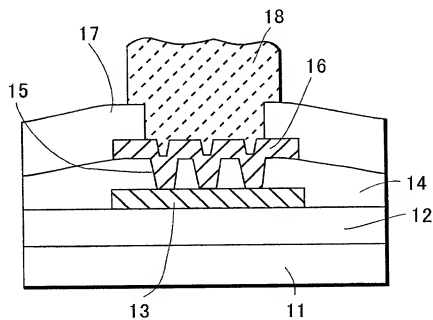


FIG. 16

